Single Thyristor, 80A

FEATURES

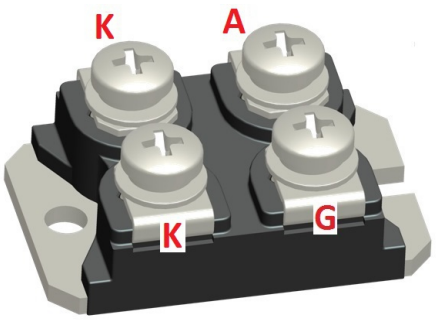
- Thyristor for line frequency
- Planar passivated chip
- Long-term stability
- Advance power cycling
- UL approved file E320098
- Compliant to RoHS

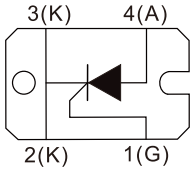
APPLICATIONS

- Line rectifying 50/60Hz
- DC Motor control
- Softstart AC motor control
- AC power control
- Power converter
- Light and temperature control

PACKAGE (SOT-227)

- Isolation voltage:3000V
- Industry standard outline
- Epoxy meets UL 94V-0
- Copper base plate, internally DCB isolated





PRODUCT SUMMARY	
$I_{T(AV)}$	80A
V_{DRM}/V_{RRM}	1200~1600 V
I_{GT}	30~100 mA

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS		VALUE	UNIT
Maximum RMS on-state current	$I_{T(RMS)}$	180° conduction half sine wave,50Hz	T_C = 80°C	125	A
Maximum average on-state current	$I_{T(AV)}$	180° conduction half sine wave,50Hz	T_C = 80°C	80	A
Maximum non-repetitive peak on-state surge current (full cycle ,T_J initial = 25°C)	I_{TSM}	F =50 Hz	t = 20 ms	1250	A
		F =60 Hz	t = 16.7 ms	1310	
Maximum I^2t Value for fusing	I^2t	t_p = 10 ms		7810	A^2s
Critical rate of rise of on-state current	di/dt	V_D = 67% V_{DRM}, t_p = 200μs, I_G = 0.3A di_G/dt = 0.3A/μs, F = 50 Hz	T_J = 150°C	150	A/μs
Peak gate current	I_{GM}	T_p = 20 μs	T_J = 150°C	3	A
Maximum gate power	P_{GM}	T_p =20μs	T_J = 150°C	10	W
Average gate power dissipation	$P_{G(AV)}$	T_J =150°C		3	W
Repetitive peak off-state voltage	V_{DRM}	T_J =150°C		1200~1600	V
Repetitive peak reverse voltage	V_{RRM}				
Maximum power dissipation	P_D		T_C = 25°C	312	W
Storage temperature range	T_{stg}			- 40 to + 150	°C
Maximum junction temperature range	T_J			- 40 to + 150	
Maximum operation temperature	T_{OP}			- 40 to + 125	

ELECTRICAL SPECIFICATIONS (T_J = 25 ºC unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		Value			Unit
				Min.	Typ.	Max.	
Gate trigger current	I_{GT}	V_D = 6V, R_L = 30Ω		30	-	100	mA
Gate trigger voltage	V_{GT}			-	-	1.4	V
Gate non-trigger voltage	V_{GD}	V_D = ⅔ V_{DRM}	T_J = 150°C	-	-	0.25	V
Gate non-trigger current	I_{GD}	V_D = ⅔ V_{DRM}	T_J = 150°C	-	-	10	mA
Holding current	I_H	I_T = 1A, Gate open		-	-	200	mA
Latching current	I_L	I_G = 1.2 x I_{GT}		-	-	350	mA
Critical rate of rise of voltage	dV/dt	V_D = ⅔ V_{DRM}, Gate open	T_J = 150°C	-	-	1000	V/μs
Forward voltage drop	V_{TM}	I_T = 75A, t_P = 380μs	T_J = 25°C	-	-	1.35	V
Off-state and reverse leakage current	I_{DRM} I_{RRM}	V_D=V_{DRM}, V_R=V_{RRM}	T_J = 25°C	-	-	50	μA
			T_J = 150°C	-	-	10	mA
RMS isolation voltage	V_{ISO}	50Hz, circuit to base, all terminals shorted, I_{ISO} ≤ 1mA	t = 1 min	2500	-	-	V
			t = 1 s	3000	-	-	
Maximum threshold voltage	$V_{T(TO)}$		T_J = 150°C	-	-	0.85	V
Maximum slope resistance	r_T		T_J = 150°C	-	-	5.5	mΩ

THERMAL AND MECHANICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUE	UNIT
Maximum thermal resistance, junction to case	R_{thJC}	DC operation	0.40	°C/W
Typical thermal resistance, case to heatsink	R_{thCS}	Mounting surface flat, smooth and greased	0.10	°C/W
Mounting force,±10% to heatsink, M4		A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound	1.1	N.m
Mounting force,±10% busbar, M4			1.1	
Approximate weight			30	g
			1.06	oz.
Case style		JEDEC	SOT-227	

ORDERING INFORMATION SCHEME

N ST 75 PT 12

Nell High Power Products

Package Indicator (SOT-227)

Current Rating

75, $I_{T(AV)}$ = 80A

Product Type

PT = Single Thyristor

Voltage Code

12 = 1200V

16 = 1600V

Fig.1 Peak on-state voltage vs. peak on-state current

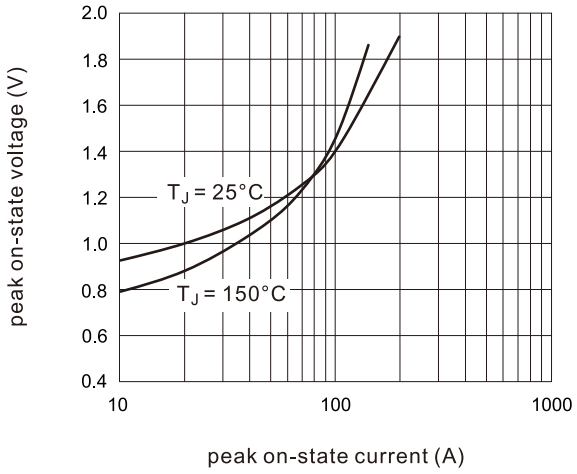


Fig.2 Max. junction to case thermal Impedance vs. time

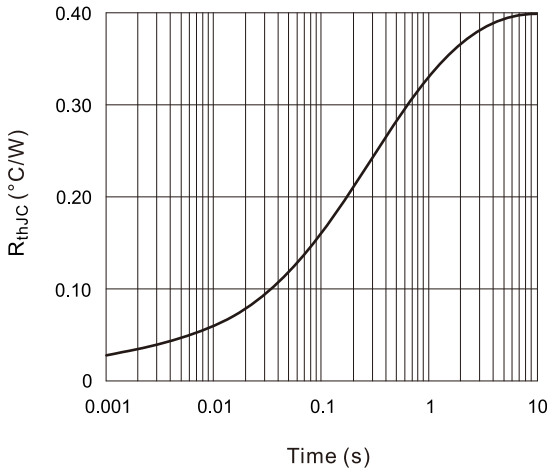


Fig.3 Power dissipation vs. average on-state current

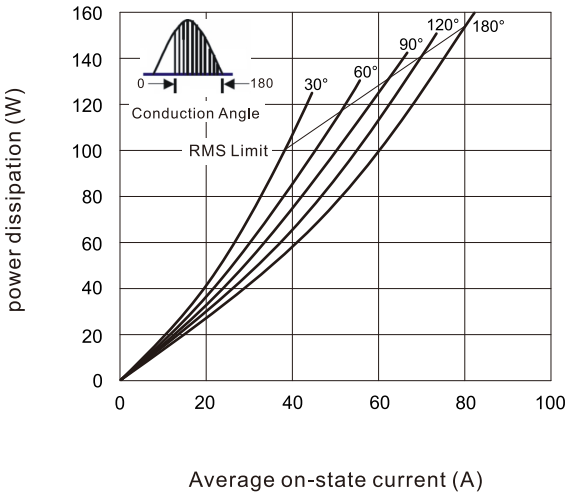


Fig.4 Case Temperature Vs. Average On-state Current

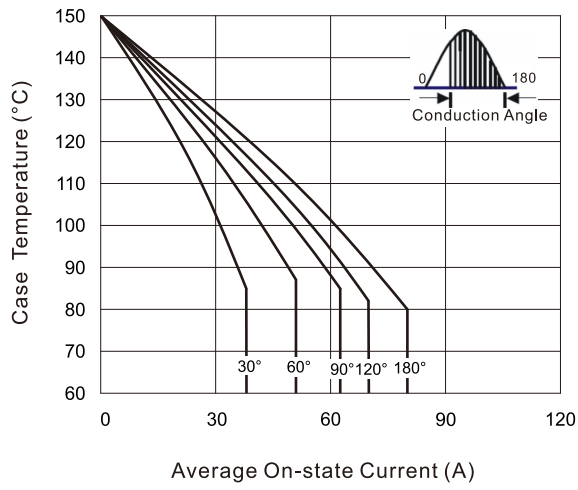


Fig.5 Surge on-state current vs. cycles

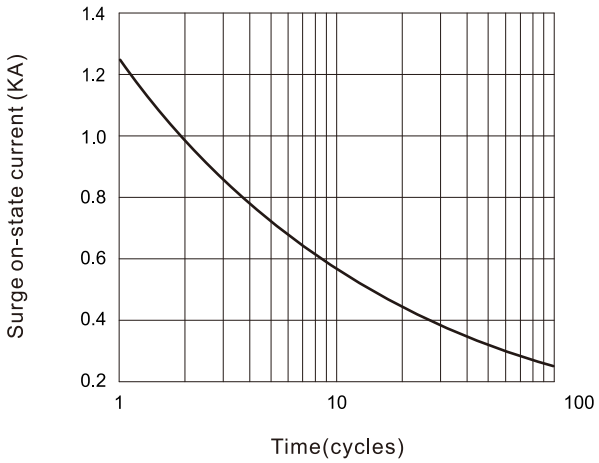
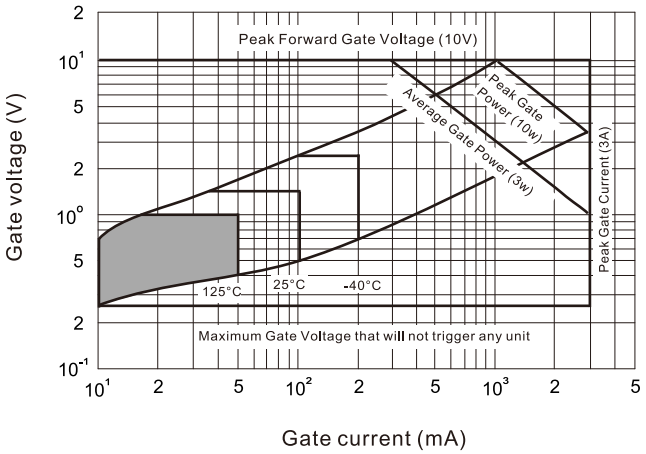
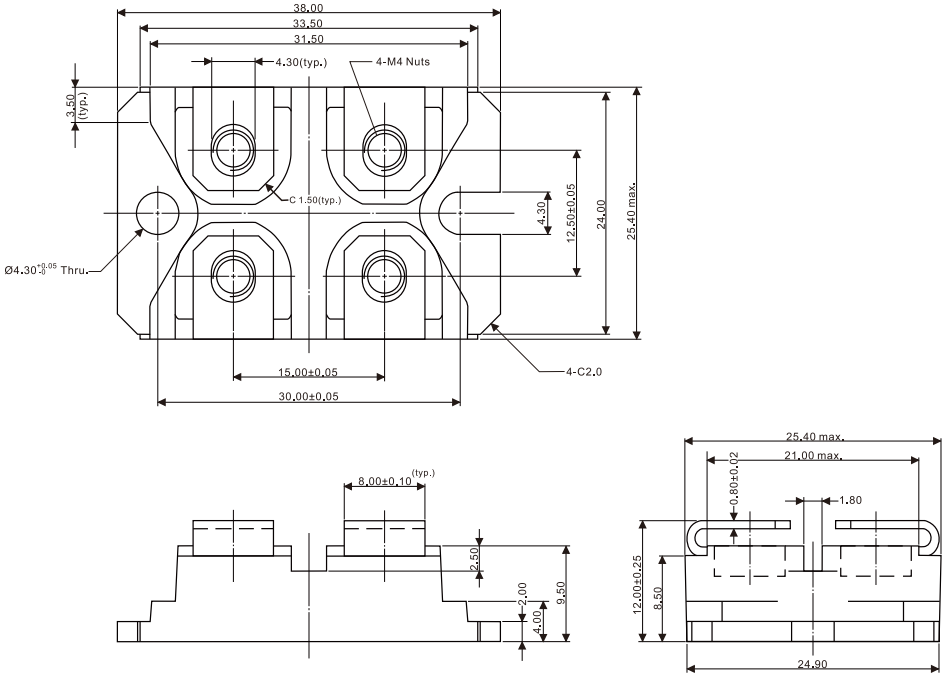


Fig.6 Gate characteristics



Case Style

SOT-227



All dimensions in millimeters